WHAT IS CLAIMED IS:

1. An electromagnetic waveform comprising a computer program, the computer program for performing formal verification of a representation of an electronic design of an integrated circuit (IC), the computer program comprising the following steps when executed by a data processing system:

conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation;

constructing a formal verification output that indicates an error if and only if an assertion is violated by a DUT/DUV and it is not the case that the assumption constraints have ever been violated.

2. An electromagnetic waveform comprising a computer program, the computer program for performing simulation verification of a representation of an electronic design of an integrated circuit (IC), the computer program comprising the following steps when executed by a data processing system:

conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation;

converting the gate-level assumption representation into a hybrid representation comprising assumption pipelines and equivalent combinational assumption constraints.

3. A method of performing formal verification, comprising:

conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation;

constructing a formal verification output that indicates an error if and only if an assertion is violated by a DUT/DUV and it is not the case that the assumption constraints have ever been violated.

4. The method of claim 3, further comprising the following step:

assuring the assumption constraints have never been violated by feeding a signal, indicative of an assumption constraint violation, through a latch circuit before combining it with a signal indicative of an assertion violation.

5. A method of performing simulation verification, comprising:

conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation;

converting the gate-level assumption representation into a representation comprising equivalent combinational assumption constraints.

6. The method of claim 3, wherein the step of conversion by logic synthesis further comprises the following steps:

conversion of declarative assumption constraints, comprising at least one sequential assumption constraint, into an HLHDL representation; and

conversion of the HLHDL representation into a gate-level representation.

7. The method of claim 5, wherein the step of conversion by logic synthesis further comprises the following steps:

conversion of declarative assumption constraints, comprising at least one sequential assumption constraint, into an HLHDL representation; and

conversion of the HLHDL representation into a gate-level representation.

8. The method of claim 5, wherein the step of converting the gate-level assumption representation further comprises the following step:

identifying deadend states.

9. The method of claim 8, wherein the step of identifying deadend states comprises the following step:

determining a deadend states set from a fail function.

10. The method of claim 8, wherein the step of identifying deadend states comprises the following step:

determining an augmented deadend states set backward from a deadend states set until a fixed point is reached.

11. The method of claim 10, wherein the step of determining an augmented deadend states set comprises the following step:

existential quantification of a variable representing an output from a design under test or verification to an environment.

12. The method of claim 8, further comprising the following step:

augmenting the equivalent combinational assumption constraints such that the deadend states are avoided.

13. The method of claim 5, wherein the step of converting the gate-level assumption representation further comprises the following step:

determining a fail function from assumption gates.

14. The method of claim 5, wherein the step of converting the gate-level assumption representation further comprises the following step:

determining a reachable states set.

15. The method of claim 5, wherein the step of converting the gate-level assumption representation further comprises the following step:

determining a valid transition function by identifying a type of transitive fanin of a register bit of an assumption pipeline.

16. The method of claim 5, wherein the step of converting the gate-level assumption representation further comprises the following step:

determining an augmented fail function using a valid transition function and a set of deadend states.

17. The method of claim 16, further comprising the following step:

augmenting the equivalent combinational assumption constraints with a constraint based upon the augmented fail function.

18. The method of claim 5, wherein the step of converting the gate-level assumption representation further comprises the following step:

identifying augmented assumption gates, as a type of transitive fanin, starting from an assumption error output.

19. The method of claim 5, wherein the representation comprising equivalent combinational assumption constraints is a hybrid representation also comprising an assumption pipeline.

20. An electromagnetic waveform comprising a computer program, the computer program for performing formal verification, the computer program comprising the following steps when executed by a data processing system:

conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation; and

constructing a formal verification output that indicates an error if and only if an assertion is violated by a DUT/DUV and it is not the case that the assumption constraints have ever been violated.

21. An electromagnetic waveform comprising a computer program, the computer program for performing simulation verification, the computer program comprising the following steps when executed by a data processing system:

conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation; and

converting the gate-level assumption representation into a representation comprising equivalent combinational assumption constraints.

22. A computer program product comprising:

a computer usable medium having computer readable code embodied therein for performing formal verification, the computer program product including:

computer readable program code devices configured to cause a computer to effect conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation; and

computer readable program code devices configured to cause a computer to effect constructing a formal verification output that indicates an error if and only if an assertion is violated by a DUT/DUV and it is not the case that the assumption constraints have ever been violated.

23. A computer program product comprising:

a computer usable medium having computer readable code embodied therein for performing simulation verification, the computer program product including:

computer readable program code devices configured to cause a computer to effect conversion, by logic synthesis, of declarative assumption constraints, comprising at least one sequential assumption constraint, into a gate-level assumption representation; and

computer readable program code devices configured to cause a computer to effect converting the gate-level assumption representation into a representation comprising equivalent combinational assumption constraints.